CLAIMS

What is claimed is:

1. A method for forming a memory device, comprising:
   providing a stacked structure on a substrate, the stacked structure comprising a first dielectric, a floating gate, a second dielectric, and a control gate;
   forming a liner dielectric layer that extends in a direction substantially parallel to the control gate on sidewalls of the stacked structure; and
   forming a barrier layer on at least part of the liner dielectric layer.

2. The method as set forth in claim 1, wherein the providing of a stacked structure on a substrate comprises:
   forming a first dielectric layer on the substrate;
   forming a floating gate on the first dielectric layer;
   forming a second dielectric layer on the floating gate; and
   forming a control gate on the second dielectric layer.

3. The method as set forth in claim 1, wherein the forming of a barrier layer comprises forming a silicon nitride layer.

4. The method as set forth in claim 3, wherein:
   the memory device comprises at least one flash memory cell;
   the method comprises implanting dopants into areas of the substrate to form source and drain regions within the substrate; and
   the method further comprises forming a silicon dioxide spacer on the silicon nitride layer.

5. The method as set forth in claim 3, wherein the forming of the liner dielectric layer comprises performing thermal oxidation such that the liner dielectric layer comprises silicon dioxide.

6. The method as set forth in claim 5, wherein the forming of the silicon nitride layer comprises chemical vapor deposition (CVD) of silicon nitride.

7. The method as set forth in claim 6, wherein a thickness of the silicon nitride layer is larger than about 30 Å.

8. The method as set forth in claim 5, wherein the forming of the silicon nitride layer comprises performing a nitridation process.

9. The method as set forth in claim 8, wherein the performing of a nitridation process comprises performing rapid thermal processing in the presence of NO, N_2, N_2O or NH_3.

10. The method as set forth in claim 9, wherein the forming of the silicon nitride layer comprises forming the silicon nitride layer to a thickness greater than about 10 Å.

11. The method as set forth in claim 8, wherein the forming of the silicon nitride layer comprises exposing the liner dielectric layer to an N_2 plasma.

12. The method as set forth in claim 11, wherein the forming of the silicon nitride layer comprises forming the silicon nitride layer to a thickness greater than about 10 Å.

13. The method as set forth in claim 1, wherein the providing comprises providing a stacked structure comprising a second dielectric, which includes:

a lower layer of insulator material;

a middle layer of charge trapping material formed on the lower layer; and

an upper layer of insulator material formed on the middle layer.

14. The method as set forth in claim 1, wherein the providing comprises providing a stacked structure comprising a second dielectric, which includes:

a lower layer of oxide;

a middle layer of nitride formed on the lower layer; and

an upper layer of oxide formed on the middle layer.

15. The method as set forth in claim 1, wherein the liner dielectric and the barrier layer are formed to extend over source/drain regions of the memory device.

16. The method as set forth in claim 1, wherein the liner dielectric and the barrier layer are formed not to extend over source/drain regions of the memory device.

17. A memory device formed on a substrate, the memory device comprising:

a stacked structure including:

a first dielectric layer disposed on the substrate;

a floating gate disposed on the first dielectric layer;

a second dielectric layer disposed on the floating gate;

a control gate disposed on the second dielectric layer;

a liner dielectric layer formed on sidewalls of the stacked structure which extend in a direction parallel to the control gate; and

a barrier layer formed on at least part of the liner dielectric layer.

18. The memory device as set forth in claim 17, wherein the barrier layer is formed to extend above an edge of the first dielectric in a direction away from the substrate.

19. The memory device as set forth in claim 18, wherein a maximum dimension of the barrier layer extends substantially perpendicularly to the substrate.

20. The memory device as set forth in claim 19, wherein the barrier layer is formed to extend in a direction that does not overlie a source/drain region of the memory device.

21. The memory device as set forth in claim 17, wherein the barrier layer is formed adjacent to an edge of the first dielectric.

22. The memory device as set forth in claim 21, wherein the barrier layer is formed to extend away from the edge of the first dielectric in a direction substantially parallel to the substrate.

23. The memory device as set forth in claim 22, wherein a maximum dimension of the barrier layer extends in a plane that is substantially parallel to the substrate.

24. The memory device as set forth in claim 23, wherein the barrier layer is formed to extend in a direction that does not overlie a source/drain region of the memory device.

25. The memory device as set forth in claim 23, wherein the barrier layer is further formed to extend above the edge of the first dielectric in a direction away from the substrate.

26. The memory device as set forth in claim 25, wherein a maximum dimension of the barrier layer extends in a direction substantially perpendicular to the substrate.

27. The memory device as set forth in claim 26, wherein the barrier layer is formed to extend in a direction that does not overlie a source/drain region of the memory device.

28. The memory device as set forth in claim 17, wherein the second dielectric layer comprises:

a lower layer of insulator material;

a middle layer of charge trapping material formed on the lower layer; and

an upper layer of insulator material formed on the middle layer.

29. The memory device as set forth in claim 17, wherein the second dielectric layer comprises:

a lower layer of oxide;

a middle layer of nitride formed on the lower layer; and

an upper layer of oxide formed on the middle layer.

30. The memory device as set forth in claim 17, wherein the liner dielectric and the barrier layer are formed to extend over source/drain regions of the memory device.

31. The memory device as set forth in claim 17, wherein the liner dielectric and the barrier layer are formed not to extend over source/drain regions of the memory device.